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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/670,194	09/26/2003	Toshio Kimura	1035-471	4479

23117 7590 04/23/2007
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EXAMINER	
IM, JUNGHWA M	
ART UNIT	PAPER NUMBER
2811	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/23/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/670,194	KIMURA ET AL.	
	Examiner	Art Unit	
	Junghwa M. Im	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *20 November 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10 and 19-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 and 19-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on October 2, 2006 has been entered.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 5-8 and 20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 5-6 recite the limitation "at least one type of the through electrodes is non-contact through electrodes not electrically connected to the electrode pad." This limitation is confusing since the all of the through electrodes are connected to a pad. Note that each of the through-holes is electrically connected to an electrode pad of at least one of the electrode formed in the semiconductor. In detail, a top of the non-contact electrode 12(1) is electrically connected to the second electrode pad in the chip [10b] through a connection to the through electrode 11(1). Claim 20 recites the substantially identical limitation in nature.

Claims 7-8 recite the limitation "a through electrode is further provided in regions outside of the electrode pad." It is confusing to understand this limitation since the instant invention does not recite this aspect.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3, 5, 7, and 19-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Tomita et al. (US 5191405), hereinafter Tomita.

Regarding claim 1, Fig. 1h of Tomita shows a chip-stack semiconductor device, comprising:

multiple semiconductor chips [1, 6, 15, 23] vertically stacked on top of each other, wherein:

each of the semiconductor chips includes electrode pads [3, 4, 11, 24, 25, 26], and

multiple through electrodes [9, 22, 27] formed in a region of the electrode pads, wherein multiple through electrodes formed in a region within the electrode pads and wherein at least two of the through electrodes formed in a region within the same electrode pad are not in direct electrical contact with each other. (Note that two through electrodes are connected to the pad 25; one from the layer 1, the one from the pad on the layer 15.).

Regarding claim 3, Fig. 1h of Tomita shows that at least one type of the through electrodes (the one connected from the layer 1) is contact through electrodes electrically connected to the electrode pad.

Regarding claim 5, insofar as understood, Fig. 1h of Tomita shows that at least one type of the through electrodes (the one connected from the layer 15) is non-contact through electrodes not electrically connected to the electrode pad.

Regarding claims 7, insofar as understood, Fig. 1h of Tomita shows that a through electrode (the second on the left) is further provided in regions outside of the electrode pad.

Regarding claim 19, Fig. 1h of Tomita shows that the electrode pads are electrically connected with a device region of the semiconductor chip.

Regarding claim 20, insofar as understood, Fig. 1h of Tomita shows a chip-stack semiconductor device, comprising:

multiple semiconductor chips [1, 6, 15, 23] vertically stacked on top of each other, and at least first and second electrodes [] provide on at least one of the semiconductor chips wherein:

each of the semiconductor chips includes through electrodes [9, 22, 27] connected to each other in regions inside of electrode pads, each of through electrodes linking a front surface to a back surface of the semiconductor chip; and

each of the semiconductor chips includes multiple through electrodes [3, 4, 11, 24, 25, 26] and wherein a plurality of different through electrodes are located inside of the first electrode pad, wherein ay least two of the through electrodes (the one from the layer 1 and the one from the layer 15) formed in a region within the same electrode [25] are not in direct electrical contact to each other.

Regarding claim 21, Fig. 1h of Tomita shows a plurality of different through electrodes (the one from the layer 1 and the one from the layer 15) provide in the first electrode pad 925), first and second of these different through electrodes carry different signals.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2, 4, 6, 8, 9-10 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tomita in view of Tsunashima (US 6087719)

Regarding claim 2, Tomita shows most aspects of the instant invention except "at least one semiconductor chip the electrode pads are provided along a periphery of the semiconductor chip so as to surround a device region." Fig. 3B of Tsunashima shows a stacked semiconductor device wherein for at least one semiconductor chip the electrode pads are provided along a periphery of the semiconductor chip so as to surround a device region.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Tsunashima into the device of Tomita in order to have the electrode pads along a periphery of the semiconductor chip for electrical connection to an outer device.

Regarding claim 4, Fig. 1h of Tomita shows that at least one type of the through electrodes (the one connected from the layer 1) is contact through electrodes electrically connected to the electrode pad.

Regarding claim 6, insofar as understood, Fig. 1h of Tomita shows that at least one type of the through electrodes (the one connected from the layer 15) is non-contact through electrodes not electrically connected to the electrode pad.

Regarding claim 8, insofar as understood, Fig. 1h of Tomita shows that a through electrode (the second on the left) is further provided in regions outside of the electrode pad.

Regarding claims 9-10, Fig. 1h of Tomita shows most aspects of the instant invention except "the through electrodes in the semiconductor chips are connected to each other via bumps so that the semiconductor chips are vertically stacked on top of each other." Fig. 1 of Tsunashima shows that the through electrodes in the semiconductor chips are connected to each other via bumps [9] so that the semiconductor chips are vertically stacked on top of each other.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Tsunashima into the device of Tomita in order to have the through electrodes in the semiconductor chips connected to each other via bumps to secure the connection

Regarding claim 22, Fig. 1h of Tomita shows a plurality of different through electrodes (the one from the layer 1 and the one from the layer 15) provide in the first electrode pad 925), first and second of these different through electrodes carry different signals.

Response to Arguments

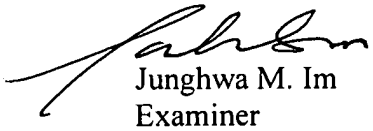
Applicant's arguments with respect to pending claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Junghwa M. Im whose telephone number is (571) 272-1655. The examiner can normally be reached on MON.-FRI. 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard T. Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Junghwa M. Im
Examiner
Art Unit 2811

jmi